

Cadence Introduces New Features for SPB 16.2

Cadence Design Systems, Inc. announces a sweeping set of improvements to the Cadence Allegro and OrCAD families of products aimed at boosting performance and productivity through new features and functionality. Part of the Cadence SPB 16.2 release, the new technology helps deliver shorter, more predictable design cycles...

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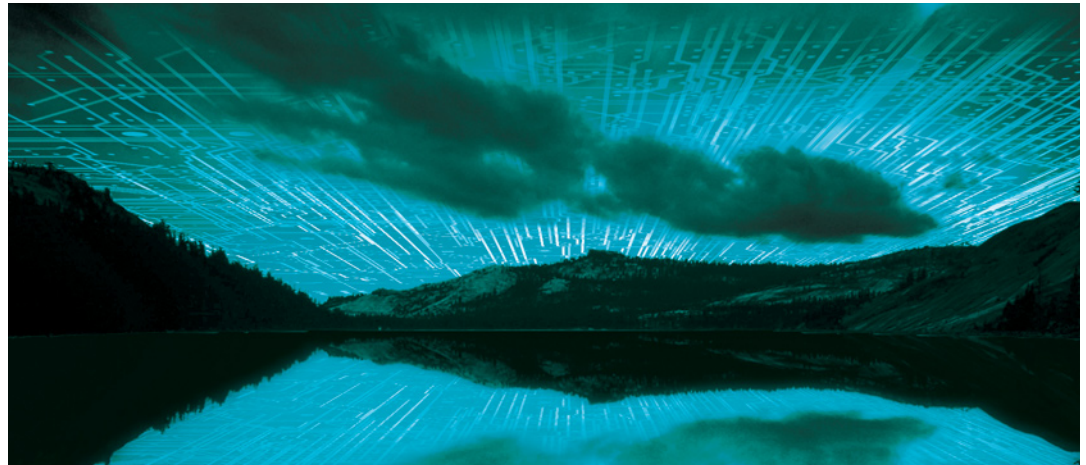
Tech Tip

Create Fanout feature in Cadence OrCAD PCB Editor
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High-Speed PCB Design

Defining and dealing with the unique challenges of high-speed PCB design
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...and Much More!



An In-Depth Look at Cadence SPB Release 16.2

By Cadence Design Systems

The Cadence® Allegro® and Cadence OrCAD® families of products for PCB design and IC packaging/SiP design provide automation, advanced codesign, and constraint-driven flows that speed product development from concept and capture to manufacturing. The latest Allegro and OrCAD release (16.2) enhances these solutions with new capabilities that address current and future business-driven technology challenges, including miniaturization, shorter product lifecycles, increasing design speeds, and environmental concerns.

Miniaturization/High-Density Interconnect

In the area of product miniaturization, significant improvements for designers using high-density interconnect (HDI) will be of particular value to customers in the high-end consumer and wireless handheld electronics market, as well as in the computing and networking segments where users are seeking a constraint-driven HDI design flow. "Cadence has excelled in constraint-driven PCB design flows for many years, but customers also increasingly demand an HDI capability," explains Keith Felton, Group Director PCB and IC Packaging Product Marketing, Cadence Design Systems. "With the significant improvements in the latest

release of our PCB and IC packaging technology, Cadence now offers both of these capabilities, and some of our customers are already seeing the benefits of our constraint-driven HDI design flow."

"Harris has worked closely with Cadence on improvements in Allegro," said Charlie Davies, Principal ECAE Application Engineer at Harris Government Communications Systems Division. "We are part of a small, diversified group of customers providing feedback to Cadence on improvements in Allegro 16.2. The biggest improvement in the Allegro 16.2 release has been in the area of designing PCBs using a build-up process with high-density interconnects. With the addition of capabilities for HDI, Allegro provides an excellent constraint-driven HDI design flow. These advances along with other ease-of-use improvements will significantly improve our ability to execute our most difficult HDI design challenges, while reducing our design cycle time."

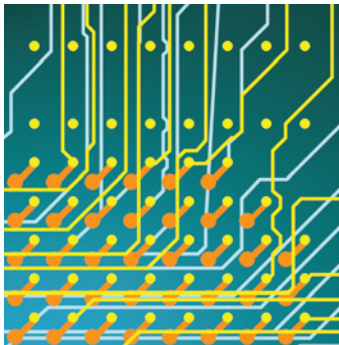
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EMA Currents

Continued from front cover

for PCB designs. With significant improvements for designers using high-density interconnect (HDI), the technology will be of particular value to customers in the high-end consumer electronics market, as well as those in segments such as computing and networking where users are seeking a constraint-driven HDI design flow.

The previous SPB 16.0 release made a significant investment in improving the ease of use of Allegro and OrCAD PCB Editor. The new 16.2 release continues this emphasis on improving ease of use for all products in the Allegro and OrCAD families, from design creation tools in the front end to PCB layout tools in the backend.



Cadence PSpice® A/D release 16.2 continues to provide user with robust and predictive simulation technology. The new release presents productivity and usability improvements including an updated GUI, new models and modeling support, and Check-Point Restart for digital and mixed signal circuits.

These are just a few of the new features and product enhancements that are available with the latest release from Cadence. For more information on SPB 16.2 visit: <http://www.ema-eda.com/new>.

Continued from front cover

Enhancements such as these make 16.2 a very important release for PCB and IC package designers. For example, the HDI capability includes new features such as enhanced design rules for microvias and same-net elements, along with powerful automation-assisted interconnect and via pattern insertion. Manufacturing IP-driven wirebonding from Kulicke & Soffa and co-planar waveguide modeling further boost productivity and reduce manufacturing-driven ECOs.

Shrinking Product Lifecycles

To deal more effectively with product lifecycle issues, the Allegro and OrCAD 16.2 release delivers features such as extended rule-driven assembly rule checking for IC packages, auto-intelligent step and repeat of complex placement patterns, and enhanced automation for PCB layout-driven RF design. It also enables IC package/SiP team-based design to reduce design cycle time and make resource usage more efficient.

Additionally, all Allegro and OrCAD products—from front-end design creation to signal integrity to backend layout—have been enhanced in the 16.2 release. One new capability enables customers to integrate RF circuits on PCBs together with digital and analog circuits. The Cadence Allegro PCB RF Option achieves this with two major enhancements: a bi-directional interface with Agilent's ADS RF design environment, and a new layout-driven RF design capability that makes it easier to modify RF circuits. The layout-driven RF design capability in the Allegro PCB RF Option also allows users to add RF circuit elements—stripline or microstrip elements—and the system will automatically create RF schematic elements through a back-annotation process. This eliminates the need for RF designers to manually create RF schematics for changes made in the layout, shortening design cycle times and reducing the risk of introducing manual errors.

The proven Cadence constraint-driven PCB design flow also provides additional control of constraints that electrical engineers need in specifying their design intent. Engineers can now specify physical and spacing constraints on critical nets and embed those in the design. These constraints are required for signals such as those found in DDRx memory interfaces, where the engineer needs to specify line widths and spacing to manage impedance and shield critical signals from crosstalk.

Cadence OrCAD Capture further delivers improved capabilities for designing FPGAs into products. Users can easily import an FPGA's pin assignment from FPGA vendor tools. It also creates split sym-

bols, and allows users to control how the symbols are split. This makes it easier to integrate an FPGA into the PCB design. Should a user choose to make changes to the FPGA pin assignment, OrCAD Capture provides the capability to export an updated pin assignment to the FPGA vendor's tool. With this release, it supports Altera and Xilinx formats for import and export. Future support for other vendors will be provided based on customer requests.

Users of the 16.2 release will also notice improvements to the graphical user interface and use models in Cadence Allegro PCB Editor as well as other Allegro and OrCAD products. Enhancements include a new application mode for placement in Allegro and OrCAD PCB editors, improved snapping capabilities with many choices on RMB, and new font support and keyboard shortcuts in Cadence Allegro Design Entry HDL.

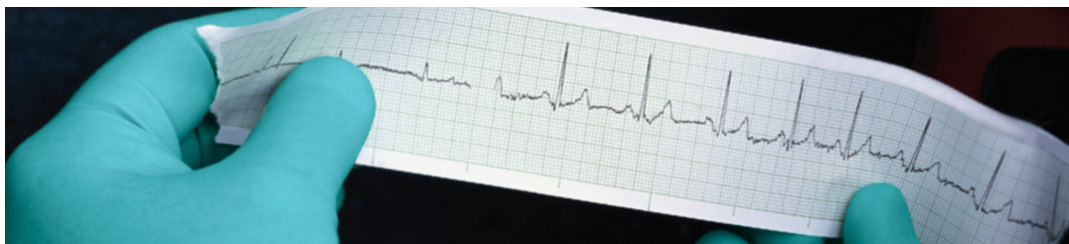
Increasing Design Speeds/Streaming Data

Streaming data enhancements to the 16.2 release also helps design teams cope with increasing design speeds. Topping the list is a new 6+Gpbs interconnect analysis feature that includes full-wave interconnect modeling to address the full range of frequencies, algorithmic modeling support (which enables interoperability of advanced SerDes models from different IP vendors during simulation of high-speed serial links), and new eye diagram mask support. An enhanced constraint-driven Allegro PCB design flow also allows engineers to specify physical and spacing rules on critical nets, thereby improving the chance of first-pass success with high-speed PCB designs by eliminating the need to communicate by email and spreadsheets.

Environmental Concerns/Green Design

With the increasing awareness of the need to develop products that help protect the Earth's climate and conserve resources, the 16.2 release helps companies go green. Design teams can make their products more efficient using new capabilities such as IC package power delivery analysis (which includes an integrated power analysis flow that is supported by 3D extraction of signal, power, and ground signals). It also includes the ability to optimize package PDN impedance voltage while minimizing voltage ripple. These and other enhancements also help co-design teams to optimize low-power system designs.

From improved high-speed flows to enhanced ease of use across the range of products, users will find a number of ways that the newest release of the Cadence and OrCAD family of products improves productivity and helps to address today's and tomorrow's critical challenges.



Is OrCAD Really Dead?

By Greg Roberts

Director of Marketing, EMA Design Automation

Recently there has been a lot of chatter regarding the future of the Cadence OrCAD product line. Some people have speculated or even suggested that “OrCAD is dead” or “Cadence is killing OrCAD.” I would like to address these rumors, but first a brief history of the OrCAD brand will put things in context.

OrCAD was originally an independent company founded in 1985. At that time, the only product produced by OrCAD was a schematic capture tool named SDT (short for Schematic Design Tool). In the early nineties, it was ported to Microsoft Windows and renamed “Capture.” In 1995 OrCAD acquired MASSTeck and its PCB layout tool, which was later re-named “Layout.” In 1998 OrCAD expanded its product offerings again by purchasing MicroSim and its analog simulation tool “PSPICE.” Although OrCAD was selling three different products, the Capture tool remained closely associated with the OrCAD name. Finally, OrCAD itself was acquired by Cadence Design Systems in 1999. Even though it has been 13 years since OrCAD started adding products to its portfolio, many in our industry believe “OrCAD” refers to a specific tool, OrCAD Capture, as opposed to the entire platform.

Getting back to the rumor, the source of it is the Cadence announcement of the discontinuation of Cadence OrCAD Layout in June 2007. March 31, 2009 will mark the end-of-support for the product. A replacement tool, OrCAD PCB Editor, was announced simultaneously. OrCAD Capture, Cadence OrCAD Capture CIS, Cadence SPECCTRA® for OrCAD, and Cadence PSPICE A/D are all integral parts of Cadence’s long-term product strategy and were not affected by this announcement. When our competitors say “Cadence is killing OrCAD,” they are letting our customers assume all OrCAD PCB Design technologies are affected, even

though the end-of-life announcement only applies to OrCAD Layout.

Cadence does not plan on eliminating the OrCAD PCB productivity tools from their line card. Many of the tools featured in this product line have become industry standard within the engineering community. OrCAD Capture is one of the most popular schematic capture tools in electronic design, with a large percentage of organizations using it as their primary design tool. Engineers know that when they need to complete a design quickly and reliably they can always turn to their OrCAD Capture software.

It would not make sense to take this technology away from our customers

that can be integrated with external systems like ERP and PLM. OrCAD Capture CIS is expanding the popularity of OrCAD Capture today and will continue to do so in the future.

Many OrCAD Layout customers have asked why Cadence decided to remove OrCAD Layout from the OrCAD PCB design flow. Although OrCAD Layout had its supporters, it did not reach the same level of popularity and dominance within the engineering community as OrCAD Capture and PSPICE A/D. Furthermore, Cadence already had a superior PCB layout tool within the powerful Allegro platform.

Cadence decided to streamline its PCB layout offerings and at the same time provide OrCAD customers with a superior and scalable PCB layout and routing solution. In addition to the improved capabilities of OrCAD PCB Editor, which features Allegro platform technology while being offered at [Continued on page 4 >](#)

Cadence OrCAD Capture CIS with Digi-Key Integration

OrCAD Capture CIS customers now have access to the wealth of engineering data offered in the Digi-Key® part database.

In today’s competitive environment where time to market is critical and electronic products have shorter life spans, companies must streamline their entire product development process. Placing parts on the design directly from Digi-Key greatly reduces the chance of costly re-spins due to wrong, obsolete, or non-compliant parts, and it reduces the administrative overhead involved in validating new part requests. Having the cost information available also assists in monitoring product production costs and therefore profitability.

“At Digi-Key, we take pride in finding new ways to provide the best service possible,” said Mark Larson, president and COO at Digi-Key. “Building on our success of having the number one website in our industry, we decided to make our web data available so that EMA could get our parts in front of engineers at the point of part selection.”

EMA integrated the Digi-Key database into OrCAD Capture CIS by creating the EMA Component Information Portal (CIP). CIP is a web-based solution that can be deployed enterprise-wide, providing access to the Component Information System (CIS) behind OrCAD Capture CIS.

For more information about EMA and the new Digi-Key integration visit: <http://www.ema-eda.com/digi-key>.

New TimingDesigner Release 9.1

In late October, EMA Design Automation™ announced TimingDesigner version 9.1, adding support for SDC which provides the ability to interface with FPGA and ASIC design flows. “Timing closure is one of the biggest hurdles a digital design team faces. By providing users the ability to generate SDC from a timing diagram, EMA is enabling design teams to move forward with confidence knowing their constraints will be representative of their original design intent,” said Manny Marcano.

TimingDesigner is the industry standard tool for interface timing design. It provides an easy to use and intuitive method for defining and analyzing interface timing requirements. The introduction of version 9.1 makes TimingDesigner the only tool that can generate SDC timing constraints from a timing diagram. This enables users to visually define design requirements and then automatically generate SDC to drive place and route.

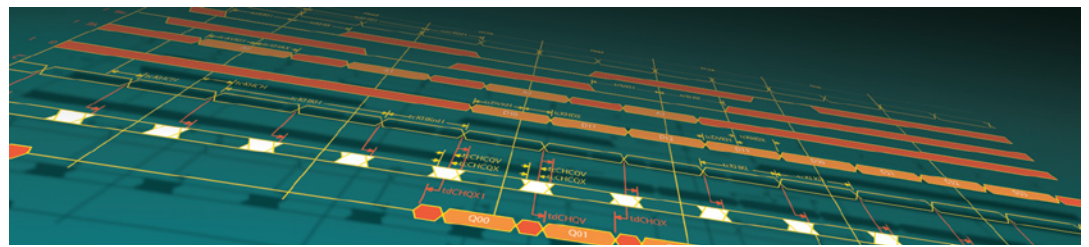
Generating SDC directly from a timing diagram removes any confusion as to the intent behind the constraints and allows users to visually debug and refine their SDC with ease. It also greatly reduces the learning curve for users new to the SDC format.

For more information on what's new in TimingDesigner release 9.1 visit: <http://www.timingdesigner.com/new>.

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prices comparable to OrCAD Layout, Cadence no longer needs to maintain different lines of PCB layout tools. Keeping PCB layout capabilities in one tool as opposed to two allows Cadence to focus its resources on designing one superior solution, improving product quality and time to market.

Some of our customers have grown to love OrCAD Layout and are not happy with the decision to discontinue it. However, the vast majority of our OrCAD Layout customers who have made the transition to OrCAD PCB Editor wish they could have taken advantage of the new tool sooner.



Using TimingDesigner to Generate SDC Timing Constraints

By Jerry Long

Application Engineer, EMA Design Automation

Introduction

As technology advances, so does the complexity of the problems it exposes. Nowhere is this more evident than in high-speed interface design. Timing issues previously deemed insignificant are now impacting design schedules and can no longer be dealt with after the fact. Design innovations such as double-data rate memory devices (DDR, DDRII, & DDRIII), with their source synchronous capabilities and continuing speed improvements, have increased the impact static timing issues have in resolving high-speed system interface operation. Margins for data setup and hold requirements are tight, which leaves minimal room to secure an accurate data capture and presentation window. Faster edge rates also magnify physical design effects, which cause signal integrity issues that require additional settling time, shrinking timing margins further.

FPGA manufacturers are keeping pace with devices that are extremely register rich and offer advanced I/O features that directly support these high-speed interface protocols. In addition, they provide intricate timing control capability with fully programmable phase-locked loop networks. These

Is OrCAD really dead? Of course not. It would not make sense to take this technology away from our customers. The messages you are receiving are the result of our competition trying to exploit the end-of-life of one tool with the hope that they can make you believe the entire product line has been affected. I am proud to say that OrCAD PCB productivity tools are alive and well and show no sign of slowing down.

features allow design of memory controllers, data exchangers, and pipeline networks, with full clock/data relationship control, dynamic termination, and I/O technology networks to comply with the latest interface styles available. While these new advances in FPGA technology are of tremendous help, they don't alleviate the importance of static timing, which if not monitored can render entire designs useless. To take full advantage of these high-performance features, you still must analyze your available timing options, incorporate signal integrity and other physical delay effects, and do so throughout the design process.

TimingDesigner® from EMA Design Automation is considered the industry standard timing analysis tool to aid in complex interface design and development as it provides an easy, self-intuitive method to address static timing issues using interactive timing diagrams. It is ideal for high-speed, multi-frequency designs where it is essential to accurately model and analyze signal relationships between devices on a board or between embedded functions on an ASIC or FPGA. It can evaluate comprehensive sets of timing alternatives and provide direction to the most complex

Continued from page 4

of timing challenges, enabling designers to manage and monitor timing margins throughout the design process. In addition, TimingDesigner can generate place and route constraints in SDC format that reference design specific timing measurements, and allows direct use of post place-and-route timing information for signal delays providing visual verification of the interface signal relationships required for desired FPGA interface operation.

Complex Interface Timing Challenges

Complex interface design presents many timing challenges, most of which aren't really new. Each device has unique data/clock relationships (i.e. edge-aligned or center-aligned) and timing requirements (i.e. input setup, input hold, and clock-to-out) for successful data operations. In order for an interface to effectively communicate data, these protocol and timing requirements must be adhered to. For FPGA and ASIC designs, these operational requirements can be referenced through the effective implementation of design constraints, the most common methodology being SDC.

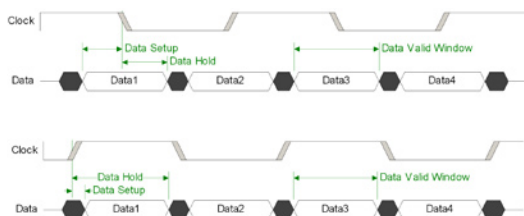


Figure 1: Examples of center-aligned (top) and edge-aligned clock/data relationships

Constraining Designs

SDC format became an open source language in 1999 for constraining complex design descriptions through synthesis, and as a result, became the defacto industry standard for ASIC and some FPGA design flows. While SDC does an effective job, there is still the complexity factor of implementing constraints correctly so that timing relationships are accurately represented. Add to that the fact that it's mostly a manual process and you end up with a constraint system that is very powerful, but at the same time susceptible to application errors and a source of confusion for correct timing analysis results. Supplying constraint information for a design basically falls into three categories of constraint commands: Clock constraints, Data constraints, and Timing exceptions.

Clock constraints are the SDC commands that specify the characteristics of all clocks used in the design. They include all characteristics of the input clock(s) (or main clock driving the design), all internally generated clock settings that are essentially derivatives of the input clock(s), and any clock(s) that are to be driven out of the device for things like source synchronous interfaces. Creating clock constraints is relatively straight forward, with minimal complexity involved, and can be used in the design implementation phase for FPGAs and ASICs as they define how certain clocks are to be treated and influence their creation.

Data constraints give relational positioning information of data signals or absolute skew requirements for any incoming or outgoing data signals for the device, and are typically referenced to a clock source. They are sometimes used in the implementation phase, depending on the complexity of the routing engines (i.e. if they take advantage of timing driven place-and-route techniques), and describe the 'boundaries' for expected fitting and routing delays. Data constraints can be quite complex due to the nature of the interface under design.

Timing exceptions are mainly to control a timing analysis engine, incorporated after the implementation phase of a design, so that the correct analysis results are calculated. These include false path controls for restricting the analysis to appropriate data paths and labeling of multi-cycle paths, all to give a more accurate and relative timing analysis result. Exceptions are not used in the implementation phase, only in the timing analysis phase.

For the complete whitepaper go to: <http://www.timingdesigner.com/sdc>.

A Closer Look: Taray 7Circuits

In April, EMA added Taray™ 7Circuits® to its comprehensive EDA software portfolio. "We can now offer our customers an integrated flow that will dramatically shorten their FPGA and PCB design cycle, and significantly improve their time to market," said Manny Marcano.

Design teams often struggle with FPGA pin assignments, employing manually-intensive methods that neglect the PCB layout until late in the design cycle. This results in increased PCB routing efforts with more layers and vias, both of which can impact manufacturing cost and signal integrity. In addition, users manually create the symbols and schematics that connect the FPGAs to the rest of the system. To insure consistency, data exchanged throughout the entire design process must be carefully managed for every change to every pin assignment on every FPGA.

7Circuits generates FPGA pin assignments that are optimized for both the FPGA and the PCB. Using its built-in FPGA library and applying a set of user-supplied constraints, 7Circuits' rule-based synthesis engine automatically creates the FPGA pin connections as well as the symbols and schematics for use by the system and PCB designers. Furthermore, it maintains this data throughout the design cycle. It also minimizes or eliminates the possibility for user-induced errors. As a result, customers can decrease their design cycles by as much as 5-15x, depending on the number of FPGAs in the design.

For more information on Taray 7Circuits visit: <http://www.ema-eda.com/taray>.

EMA Trade Shows

DesignCon 2009

Santa Clara, CA – Feb 2-5, 2009
This exhibition will feature leading organizations presenting EDA tools, PCBs and related technologies, signal integrity and design verification technologies, and more. This event presents a unique opportunity to discuss the latest design challenges while networking with innovative industry leaders. Learn more about DesignCon 2009 at: <http://www.designcon.com/2009/>.

High-Speed PCB Design On-Demand Seminar

See firsthand how the Cadence high-speed PCB design flow addresses the challenges of designing the system interconnect of today's complex designs. Discover how the Allegro system interconnect design platform enables you to manage high-speed constraints, identify and address signal integrity issues throughout the entire design process. Learn how to manage high-speed properties and automate component placement.

Who Should Attend

- Electrical engineers
- Engineering managers
- System designers
- Hardware designers
- PCB designers
- SI engineers

For access to the on-demand seminar visit: <http://www.ema-edu.com/seminars>.

My Conversion from Cadence OrCAD Layout to Cadence OrCAD PCB Editor

By Mike Moore

Technical Support Specialist, EMA Design Automation

I started my career in EDA twelve years ago at OrCAD supporting the OrCAD Layout product. Over the years I have become very proficient with this software. Until recently I believed OrCAD Layout to be the best and easiest to use PCB tool on the market for anything but the most complex boards. Then Cadence Design Systems, Inc. announced the end-of-life of OrCAD Layout.

My first thoughts were the typical emotions that come with change; frustration at losing my favorite tool, a new insecurity in my job position, and a general fear of the unknown. It came down to the fact that I knew very little about the replacement product, OrCAD PCB Editor or the Allegro platform from which it was derived. Realizing I had no choice, I dove into this software to see for myself if it could reach the pedestal on which I had placed OrCAD Layout.

It took me one week of training on OrCAD PCB Editor to realize that issues I ran into while learning the tool were the same as those I experienced while learning OrCAD Layout; bringing a netlist from the schematic onto the board, placing and routing the board, and creating gerbers. The vast majority of so-called "problems" with OrCAD PCB Editor involve learning the specific details of the program, which is the case with any new product, including OrCAD Layout.

When transitioning to OrCAD PCB Editor, many engineers go through a phase where they ask, "How do I find what I want to do?" followed by a stage of realization, "This tool has functionality I never thought was possible." OrCAD Layout has a small set of tasks it can perform compared to the more powerful OrCAD PCB Editor. As a result, engineers familiar with OrCAD Layout have a tendency to initially feel overwhelmed with additional functionality. Once the user realizes how easy this technology is to use and experiences the power of the additional capabilities, they become impressed by the tool and committed to the upgrade.

Designers will immediately benefit from two of the most important features in OrCAD PCB Editor not present in OrCAD Layout; the Constraint Manager and Padstack Designer. The Constraint

Manager allows the user to define their design, physical, and spacing constraint rules in an easy-to-use spreadsheet environment. The Constraint Manager also allows constraints to be exported from one design to another, saving valuable set-up time for the engineer.

The Padstack Designer allows users to easily create and/or edit library and design padstacks using a graphical user-interface. This feature allows users to define the different physical padstack pads, as well as thermal and anti-pad size/shape parameters. The padstack layer information can be easily added, copied or deleted, again saving the engineer valuable time. Both of these features, along with several features not mentioned, illustrate why engineers are coming to realize the value of this product.

An engineer can not expect to use OrCAD Layout for 5 or 10 years and then master OrCAD PCB Editor in just three weeks. It is easy to forget the time and effort that was necessary to reach the level of proficiency with the software platform they use today. Engineers may experience difficulty utilizing this tool by learning through self-guided trial and error. EMA offers various options to aid in the training process, including iTrain, classroom training, interactive web demonstrations, and there is always the Technical Support team. Engineers who understand they need to engage in training are the first to experience the benefits of OrCAD PCB Editor.

It all comes down to this: the overwhelming majority of engineers who are proficient with both tools have come to favor OrCAD PCB Editor; not only for its higher-level functionality, but for its ease of use. I include myself in this group. Engineers who decide, "This product is too different. I wish it worked exactly like OrCAD Layout did," struggle with the transition and fail to understand the advantages of the new technology. Engineers who decide, "I want to work with this software and understand the additional capabilities it offers," are advancing their design quality and output capacity. The engineers experiencing OrCAD PCB Editor's benefits are focused on using the tool to find solutions.

How to Embed BSDL File Names in the Board Schematics and Netlist with Cadence OrCAD Capture

By David Muse
Engineering Manager, Corelis Inc.

Introduction

Boundary-scan (IEEE standard 1149.1, also known as JTAG) uses dedicated test logic built into the components to support board level testing and in-system programming. Boards can be tested for structural and functional integrity, device interconnection, memory operation and basic functionality. Manufacturing faults such as solder bridges or open connections between devices are detected and diagnosed down to the device and pin level.

One common misconception about boundary-scan test is that it is completely the responsibility of the test or manufacturing department. During the schematic entry phase of board design there are many steps that can be taken to ensure proper operation of the JTAG chain and maximize the boundary-scan test coverage of the board. One such step is embedding the information about the Boundary Scan Description Language (BSDL) file used for each boundary-scan-compatible component in the target board's schematic and the resulting netlist.

This article explains how to use the OrCAD Capture program to embed the BSDL file names in the schematics. The BSDL file name and package information will then be included in the *packages* section of a Telesis format netlist when it is created by OrCAD Capture.

Why Embed BSDL File Names in the Netlist?

BSDL files describe how the boundary-scan interface is implemented inside the device. The automatic test pattern generation (ATPG) software uses the BSDL files and the board netlist to create the boundary-scan test vectors that are executed on the target board to detect and diagnose manufacturing faults. By including the BSDL file names in the netlist, a higher level of integration is achieved between OrCAD Capture and the ATPG tool. This allows the boundary-scan test vector generation to become more efficient through a higher level of automation.

Additionally, by forcing themselves to consider some of the design constraints required for optimal boundary-scan testing up front, the board designers can make changes before going to layout. Unlike in-circuit testers (ICTs), boundary-scan design problems cannot be resolved by simply adding a few more test points to the board. Board designers should not consider this as extra work because they can take advantage of the boundary-scan tests themselves when bringing up and debugging their prototype boards.

Editing the Schematic Symbol Properties to Include the BSDL File Name

The following example provides detailed instructions for embedding the BSDL file names in the schematic design.

1. Within OrCAD Capture, highlight the schematic symbol of a boundary-scannable component
2. Right click and select **"Edit Properties,"** as shown in Figure 1

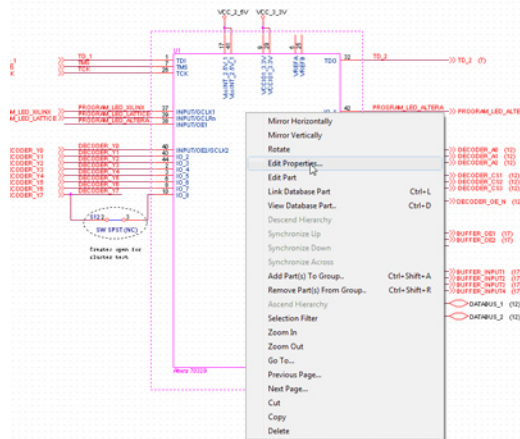


Figure 1: Editing the Schematic Symbol Properties

3. Add a new column to the property editor by clicking on the **"New Column"** button. In the resulting dialog box, add a column called **"BSDL File,"** as shown in Figure 2
4. For each boundary-scan-compatible device, go to the property editor and add the BSDL file name to the **"BSDL File"** column

NEW! Interactive Web Demonstrations

EMA has developed an exciting new series of interactive web demonstrations! This series focuses on taking your PCB designs from concept through production. Using Cadence PCB design technologies, these web demonstrations address issues experienced throughout the entire PCB design flow. Attend our new web-based demonstration series that illustrates this complete solution and incorporates additional EDA technologies that supplement the Cadence PCB design flow.

Featured Interactive Web Demonstrations

- Designing with Cadence OrCAD Capture
- Migrating Designs to Cadence OrCAD PCB Editor
- Preparing PCB Designs for Manufacturing
- Cadence PSpice Advanced Analysis - Automatically Fine-Tune Your Circuits
- Cadence Allegro Design Entry CIS Integration with Cadence Allegro PCB Editor
- Migrating Designs to Cadence OrCAD PCB Editor
- Accelerating FPGA and PCB Design with Taray 7Circuits

For the complete list of demonstrations visit: <http://www.ema-eda.com/demos>.

Next Generation Virtuoso Custom Design Platform

In late September, Cadence Design Systems, Inc., the leader in global electronic design innovation, announced the availability of the latest update (IC 6.1.3) to its next-generation Cadence Virtuoso® custom design platform. Cadence continues to provide a complete solution enabling customers to design custom integrated circuits reliably and with a high level of productivity. This latest release incorporates new technology as well as significant performance improvements in existing technology, offering advanced solutions for the custom design of chips proven in production by dozens of customers.

“We added significant performance-enhancing capabilities to the Virtuoso platform’s IC 6.1.3 release that enable customers to boost productivity while delivering their complex products on schedule and with high reliability,” said Srinivas Raman, Corporate Vice President of Research and Development at Cadence Design Systems.

A new design-centering flow enables customers to measure and refine their circuits, and increase their confidence that those circuits meet predicted yield targets. This flow is further enhanced by a unique integration of the Virtuoso Multi-Mode Simulation engines with the Virtuoso Analog Design Environment XL, providing customers with up to three times the interoperability performance gain.

For more information on the Virtuoso platform visit: <http://www.ema-eda.com/virtuoso>.

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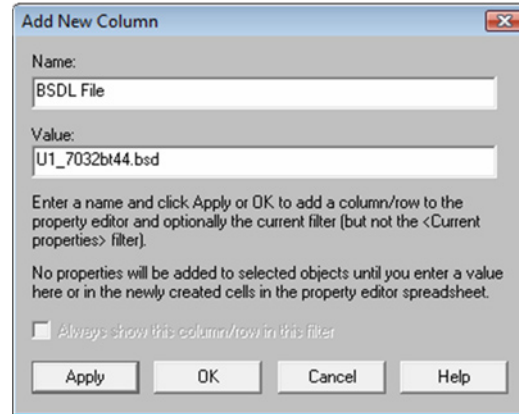


Figure 2: Add New Column Dialog

5. Also add the package designation as it appears in the BSDL file to the “PCB Footprint” column, as shown in Figure 3

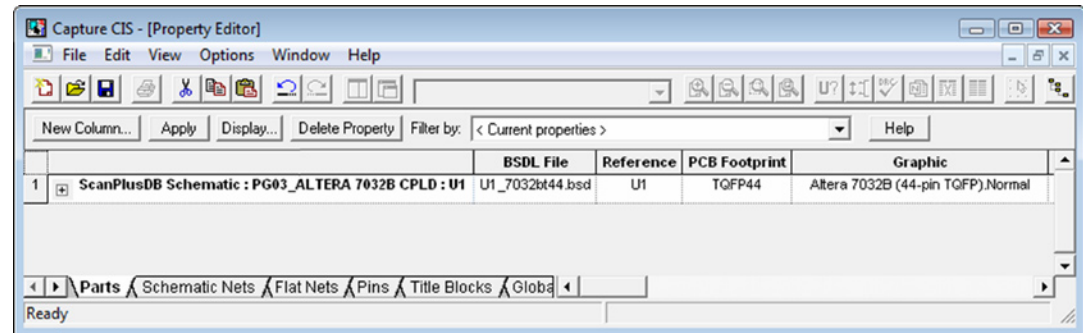


Figure 3: Property Editor

6. The values for the “BSDL File” name and “PCB Footprint” can be displayed on the schematic page by setting the “Visible” property for each value. An example schematic symbol with the BSDL file name displayed is shown in Figure 4

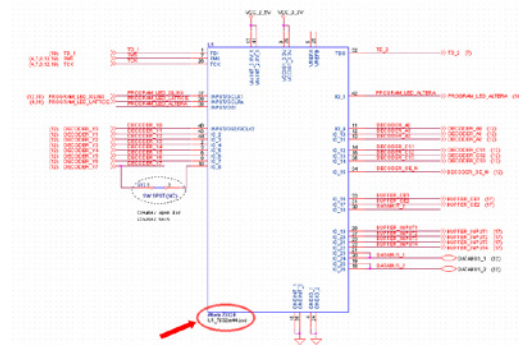


Figure 4: Example Schematic Symbol with BSDL File Name Visible

Now that the BSDL file information is present in the schematic design the netlist can be generated.

Generating the Netlist

The following steps describe how to generate a Telesis format netlist with the BSDL file information embedded in the packages section:

1. Within OrCAD Capture, select the top level design in the project manager and make sure that design is displayed in “Physical” mode
2. Select “Create Netlist” from the “Tools” menu
3. Select the “Allegro” tab and the “Telesis” format in the “Create Netlist” dialog that comes up
4. Add the “BSDL File” field to the “Part Value” combined property string as shown in Figure 5. The “{}” brackets are required. The “[]” brackets are optional but their use makes the information in the netlist easier to read. Please note there is a space between the {Value} string and the next bracket

5. Specify the desired output file name in the “Netlist File” text box. Figure 5 shows an example after these steps have been completed

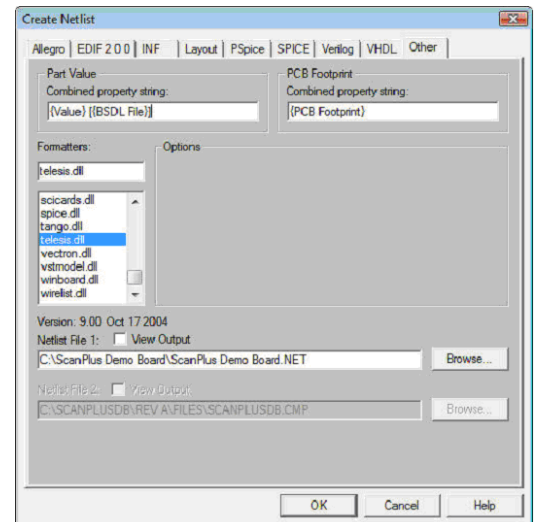


Figure 5: Create Netlist Dialog

6. Click the “OK” button to generate the netlist. Figure 6 shows an example netlist in Telesis format generated with embedded BSDL file information

Continued from page 8

```

$PACKAGES
'1.0K_RPK'      ! '1.0K_RPK'                      ; RN4
'4.7K_RPK'      ! '4.7K_RPK'                      ; RN5
'TQFP44'        ! 'ALTERA_7032B                    [7032bt44.bsd]' ; U1
'FG256'         ! 'XILINX_XC2S50                    [XC2S50_fg256.bsd]' ; U2
'TQFP_100'      ! 'LATTICE_MACH_M4A3                [M4A96t.bsd]' ; U3
'BGA_316'       ! 'POWERPC405                       [IBM25PPC405CR.BSD]' ; U4
'VQ44'          ! 'XILINX_9536XL                   [XC9536XL_vq44.bsd]' ; U5
'20PIN_SOIC'    ! '74LVC244                         ; U7

$NETS
MY_NET1 ;      U17.34 U54.AA12 U13.3 R2.1
FLASH_CS- ;    U53.91 U40.M5

$END
    
```

Figure 6: Example Telesis Netlist with Embedded BSDL File Names

Boundary-scan Test Vector Generation Automation with Corelis ScanExpressTPG

Embedding the BSDL file name information in the netlist enables the boundary-scan test vectors to be generated much more quickly and efficiently. Corelis ScanExpressTPG (SETPG) is a program that creates boundary-scan test programs and test patterns using the board design netlist and the BSDL files. SETPG reads the BSDL file name information from the netlist and automatically matches the reference designators of the boundary-scan compatible devices to the corresponding BSDL files in the project directory. Simply click the **“Auto-Find”** button and ScanExpressTPG determines the boundary-scan chain configuration without any further user interaction. A sample boundary-scan vector generation project screen is shown in Figure 7.

Conclusion

By embedding the BSDL information in the schematics and netlist, a design engineer can greatly increase the integration between the OrCAD Capture application and the ATPG software used to generate the boundary-scan test vectors. By taking the time to provide this information, designers can leverage the automation features in the boundary-scan tools to shorten their own board bring-up and debugging time and allow the manufacturing and test departments to be more efficient.

For more tips and general guidelines about how the OrCAD Capture application can be used to design boards that are more testable using boundary-scan, please visit: <http://www.corelis.com/Board-Design.htm>. A complete white paper covering board design for boundary-scan testability is also available at: http://www.corelis.com/DFT_White_Paper_Request.html. There is a tutorial on boundary-scan itself at: http://www.corelis.com/products/Boundary-Scan_Tutorial.htm.

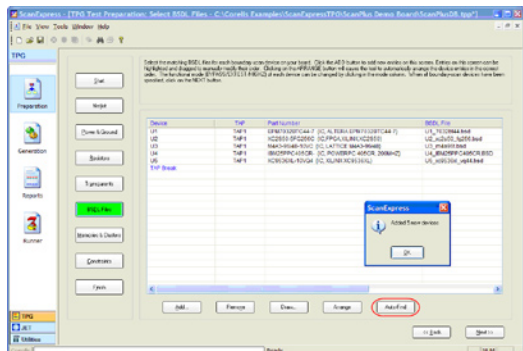


Figure 7: Corelis ScanExpressTPG Scan Chain Configuration Automation

CircuitSpace Foundation with Cross-Probing

CircuitSpace® Foundation with Cross-Probing combines many of CircuitSpace’s feature rich capabilities, such as auto-clustering and checkpoint compare reporting, with the new Cross-Probing technology.

“We have worked closely with our key customers in developing this new technology”, stated David Ringer, Principal Product Engineer of DesignAdvance®. “Our customers have been actively deploying the solution throughout the PCB design process, providing PCB Designers, Hardware Engineers, Test Engineers, and Manufacturing Engineers a valued mechanism for design, review verification, and test.”

The new Cross-Probing technology allows the user to have bi-directional communication between layout and a (PDF) schematic. The new technology works seamlessly within the Allegro platform and the Cadence Allegro Physical Viewer environment, and gives both designers and engineers instant selection and verification of design elements such as components, nets, or pins.

Features and Capabilities:

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- Intelligent physical design reuse
- Define and save physical design templates
- Automated product change report between layout designs
- Concurrent layout development corporate wide
- Template generation for global library usage across divisions

For more information visit: <http://www.ema-eda.com/circuitspace>.

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TimingDesigner Design Kit Demonstration

This on-demand demonstration explains what TimingDesigner Design Kits are and features a demonstration on the benefits of turning a static PDF into an interactive timing model.

Enhanced Functional Verification using Cadence Incisive Platform

This introductory archived webinar illustrates a variety of solutions to address the problems in functional verification and assertion-based verification (ABV).

Managing Electrical Constraints in Allegro Design Entry CIS

This recently updated archived webinar provides in-depth consideration on topics that are essential for efficient management of design rules and constraints that often begin with Allegro Design Entry CIS

Create Fanouts in Cadence OrCAD and Allegro PCB Editors

By Walt Pyska

Technical Support Manager, EMA Design Automation

The Create Fanout feature, contained in the OrCAD and Allegro PCB Editor route menu, shown in figure 1, draws a connect line and via out from surface mount pins on a component so the connection to the pins can be made at any layer.

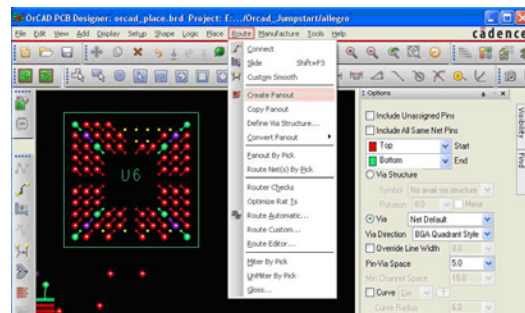


Figure 1

Additionally, this feature allows the user to generate package controls using a wide variety of control options. Some of these control options are:

- Fanout unassigned pins
- Set the line width of the fanout trace to override the minimum line width setting
- Set pin to via spacing regardless of DRC, including negative values which result in a via in pad
- Build a via structure (SMD pad to BVia to thru via) and reuse this structure when creating a fanout
- Set via types and directions, and control custom directions
- Create curved fanout

Unlike Fanout By Pick, Create Fanout is not DRC aware and may result in via to element conflicts. Running additional passes with parameter adjustments may be required to reach the user's final intent.

Another offering provided within the route menu of OrCAD and Allegro PCB editors is the Copy Fanout feature, shown in figure 2.

Using this feature, fanouts can be copied based on device type or package name. This allows the user to create one custom fanout and then rapidly duplicate that custom fanout across the design. Copying a fanout automatically replaces any

existing fanout on the chosen component unless the fixed property has been assigned or the fanout is routed to a different component. Copied fanouts replicate the origin symbol attributes, such as line width, via type, direction, or via structure. DRCs may occur after the command is completed; for example, the copied fanout via may conflict with an adjacent pad or may not meet minimum line width requirements.

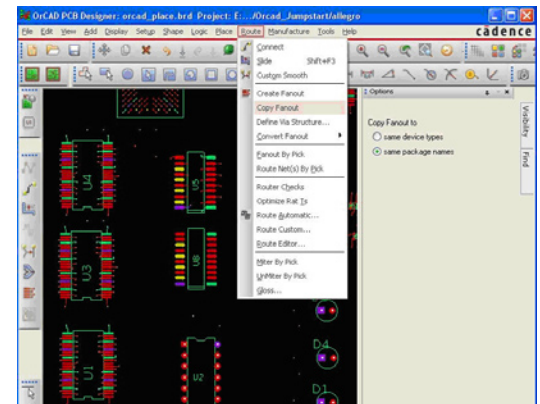
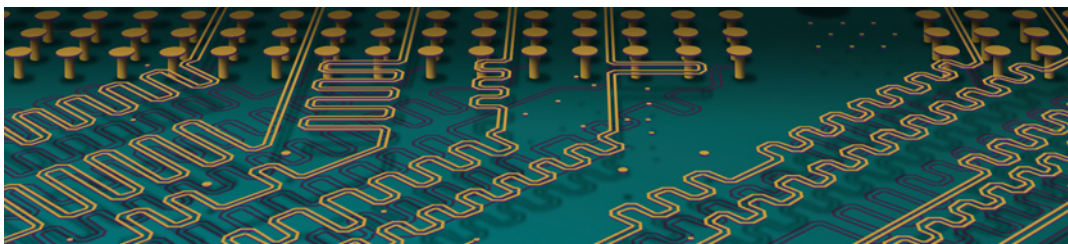


Figure 2

Additional features present in these programs include Define Via Structure and Convert Fanout. A via structure is a series of vias and clines used primarily on HDI designs to transition a signal from the surface into the HDI or core layers. The Define Via Structure feature can be used to define a combination of these elements spanning many layers.

The Convert Fanout feature is used to associate fanouts that may have originated from Cadence Allegro PCB Router or fanouts that were routed manually. Fanouts created with the interactive suite are automatically associated to the symbol instance. This feature is beneficial when moving a component; fanouts not associated remain in place when a component is moved.

The full application note containing detailed information about "Creating Fanouts in Cadence OrCAD and Allegro PCB Editors" is available at: <http://www.ema-eda.com/fanout>. The material in this application note, including step-by-step instructions on how to use these features and a sample board file, was provided by Cadence Design Systems.



High-Speed PCB Design: What Does It Mean to You?

By Bill Wiersma

National Sales Manager, EMA Design Automation

Technology continues to march forward, resulting in design implementation that uses higher and higher operating frequencies and lower power devices. As we design our next generation PCBs or systems we need to ask ourselves, "Am I designing a high-speed PCB and should I do anything different?"

Before that question can be answered, a common definition of what constitutes a high-speed PCB design needs to be agreed upon. Over the years you've likely heard various definitions ranging from, "High-speed isn't measured by frequency, its measured by rise time" or "Any signal where the round trip delay is greater than twice its edge rate." etc. How do these definitions relate to your day-to-day activities? They don't. What is needed is a relevant and practical definition that has meaning for everyone involved in the design of the PCB or system.

A pragmatic definition could be "a signal is considered high-speed when you must do something other than simply route it in an arbitrary manner." In other words, if a simple pin to pin connection is all that is needed, it is not a high speed signal. Therefore, if how a pin-to-pin trace is routed is important, then it must be controlled or constrained. Assuming you agree with this definition, what are its implications? How could it impact your day-to-day activities?

In PCB layout, these constraints are communicated as numbers (i.e. minimum or maximum trace lengths, maximum parallel lengths, etc.) This is not a new concept; we are used to working with constraints already (trace width and spacing are constraints). We also have placement constraints that are driven by the assembly process. These are traditionally regarded as physical constraints. These new constraints are called "electrical" constraints, and are communicated in terms of

length (maximum length = 1300mils) or time (maximum length = 1.2ns).

The question now is where do these constraints (or numbers) come from? There are three sources of constraints:

1. Specifications: These are normally supplied in the form of PCB layout guidelines and are supplied by the IC manufacturer. These devices are simulated and characterized by constraints and routing topologies, that are developed and sometimes distributed in the form of reference layouts. Since these constraints must work "in all cases," they are usually conservative.
2. Rules of Thumb: As the name implies, they are good layout practices, the result of years of PCB layout. Like the specifications detailed above, they are usually conservative as well.
3. Analysis: In this case, analysis or simulation is performed prior to layout. Constraints and routing topologies are then developed. These constraints are tailored to a specific design.

To dig deeper into this subject, let's use a common example of routing a differential pair. We all know that both traces of a differential pair should be the same length. One applicable rule of thumb states that an equal number of left and right turns are needed when routing a differential pair. By analyzing this rule we see that making a left turn leaves the trace on the left shorter than the right. Therefore, to equalize the length the designer must simply make a right turn. Sometimes this rule cannot be met; what then must be done? What is the maximum length differential or "phase tolerance" that a particular differential pair can tolerate and still meet the specifications as supplied by the IC manufacturer? Once again, a rule of thumb could be applied, so we could enter 100mil.

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- Reduce time and cost associated with new part approvals
- Eliminate unnecessary time that engineers spend researching component data in ERP/PLM systems

For more information contact:
info@ema-eda.com.

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Next we need to determine if there is a minimum or maximum length constraint for the differential pair. The length is determined through a combination of timing analysis and signal integrity analysis. First, timing analysis of the circuit will determine the minimum or maximum length of the differential pair. Timing analysis will determine the maximum "slack" that could be tolerated while still maintaining a functioning circuit. For example, the timing analysis reports that the signal has a slack time of 2.75ns, meaning that the signal must propagate down the trace in less than 2.75ns. If your layout system supports the specification of length in "time," then 2.75ns would be entered as the constraint. If you must specify length in "distance," it must be translated to mils or mm. You could apply a "flight time" rule of thumb or run a simulation to translate "time" into length. By applying "flight time" an approximation can be determined, but to calculate the exact length the physical board stack-up and dielectric constants are needed.

Timing analysis does not take into account the effects related to changes in rise/fall time due to signal integrity. Once again, this could be dealt with by building in an arbitrary allowance for these effects or simulating the trace to determine the impact. In either case the 2.75ns would be decreased to ensure proper operation of the high-speed PCB.

Today, many companies perform basic signal integrity analysis. Traditionally this is performed after the layout has been completed. In these situations, a rudimentary set of constraints are validated (minimum rise time, over/undershoot) to determine if the design needs to be modified. This is a workable, albeit incomplete, solution for designs with a small number of high-speed signals. As the number of high-speed signals increases, a constraint driven layout flow that leverages constraints determined before the layout is needed. This flow can eliminate errors due to timing and signal integrity by preventing them from being implemented during the layout phase.

It is clearly seen that high-speed PCB design demands a constraint driven PCB flow to ensure a high quality design. This flow will have an immediate impact on the day-to-day tasks during the design and implementation of a high-speed PCB design. The constraints are developed from a variety of sources, and timing and signal integrity analysis will be required to produce a complete set of constraints.

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